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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF: Sundar NARAYANAN, et al. ART UNIT: 2813
SERIAL NO.: 09/975,257 EXAMINER: David L. Hogans
FILING DATE: October 12, 2001
FOR: RADIATION-SENSITIVE RESIN COMPOSITION

DECLARATION UNDER 37 C.F.R. § 1.131

We, Sundar Narayanan and Krishnaswamy Ramkumar, do hereby declare and state that:

1. We are the inventors of the subject matter claimed in the above-identified application.

2. Prior to July 12, 2001, we completed our invention as described and claimed in the above-identified application in this country as evidenced by the following:

a. Prior to July 12, 2001, having earlier conceived the idea of a method of determining the nitrogen content of a nitrided gate oxide layer on a semiconductor substrate, we carried out an experiment in which a silicon wafer was placed in a furnace and a blanket thermal oxide layer was formed thereon. The thermal oxide layer was then nitrided in a furnace using nitric oxide (NO) gas. A thickness of the nitrided oxide layer was then measured. The nitrided oxide layer was then oxidized in a furnace using oxygen gas. The film thickness was again measured, and the change in thickness as during reoxidation was calculated. It was then possible to determine if the measured thickness of the oxidized nitrided gate oxide layer exceeded a target thickness value. This is described in our specification and is evidenced by the invention disclosure attached hereto as Exhibit A, which was forwarded to our attorneys at Piper Rudnick LLP at 1200 Nineteenth Street, NW, Washington, D.C. 20036, prior to July 12, 2001.

3. Each of the experiments carried out in the attached Exhibit A was performed in our laboratory in San Jose, California.

4. Each of the dates deleted from attached Exhibit A is prior to July 12, 2001.

5. All statements made herein of our own knowledge are true and all statements made on information and belief are believed true. Further, we are aware that willful false statements and the like are punishable by fine, imprisonment or both under 18 U.S.C. §1001, and that such willful false statements may jeopardize the validity of the above-captioned patent application, and any patent to issue thereon.

Date: 9/27/04

N. Sundaram

Sundar Narayanan

Date: 9/27/04

Kramkumar

Krishnaswamy Ramkumar

EXHIBIT A

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CYPRESS SEMICONDUCTOR INVENTION DISCLOSURE FORM

The description of invention should be written in the inventor's own words and generally should follow the outline given below. Sketches, prints, photos, and other illustrations, as well as memos or reports of any nature in which the invention is referred to, if available, should form a part of this disclosure and reference can be made thereto in the descriptions of the invention's construction and operation.

Problem : Currently nitrided Gate oxides are grown by nitriding a dry or wet oxide using nitriding gas anneal, which incorporates nitrogen into the gate oxide. We need a SIMS analysis to verify the % Nitrogen. The process cannot give a pass fail answer to the amount of nitrogen present in a manner amenable to manufacturing and Statistical process control. It is also a costly process.

Solution : We can do a second oxidation of the nitrided oxide as part of the same recipe at 900 to 1025 C for upto 10 minutes in pure oxygen ambient. The thickness increase is 0-8 A in case of the nitrided oxide and is three to four times this number for non-nitrided oxide. The measurement after the GOX step can clearly indicate both the GOX thickness and the Level of nitridation and give a pass/ Fail criteria.

Advantages :

The second oxidation can be done as part of the recipe in the same tool as the anneal and give a pass fail criteria.

It can be done in a separate tool to get the measure of Nitridation very accurately.

It helps improve the carrier mobility because it pushes the nitrogen away from the gate oxide silicon interface and improves electrical properties.

We can do SPC on the % Nitrogen and nitriding efficiency.

Inventor(s) N. Sundararaman Date [redacted]

Inventor(s) Krawczelly Date [redacted]

Inventor(s) ______ Date ______

Witnessed, Read, and Understood by: ______ Date ______

Witnessed, Read, and Understood by: ______ Date ______

(Each page upon which information is entered should be signed and witnessed.)

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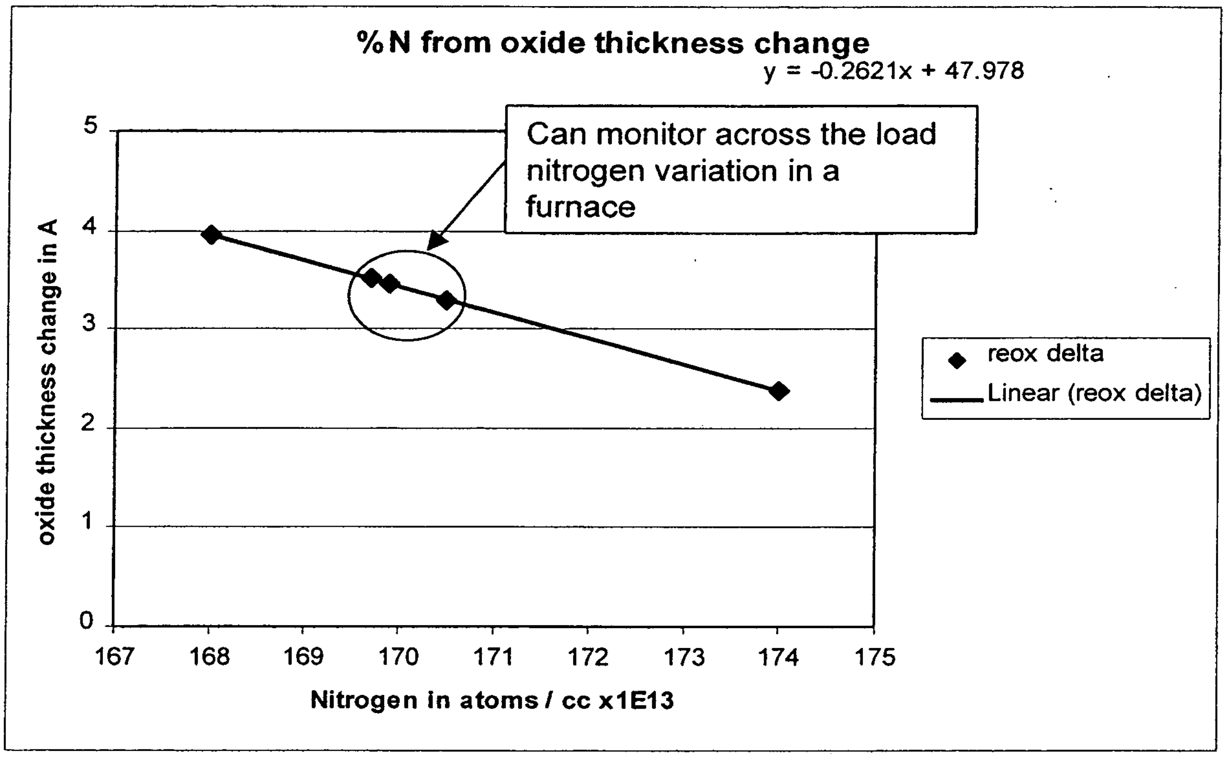
CYPRESS SEMICONDUCTOR INVENTION DISCLOSURE FORM

(INSERT ADDITIONAL INFORMATION)

Wafer description	Before 2nd oxidation	After 2nd oxidation
With Nitrogen	22.43 A	26.6 A
Without Nitrogen	23.19 A	**101.10 A**



Inventor(s) N. Sundaram Date [redacted]

Inventor(s) Krassue Date [redacted]

Inventor(s) ______ Date ______

Witnessed, Read, and Understood by: ______ Date ______

Witnessed, Read, and Understood by: ______ Date ______

(Each page upon which information is entered should be signed and witnessed.)

A NOVEL SELF MONITORING PROCESS FOR ULTRA THIN GATE OXIDATION

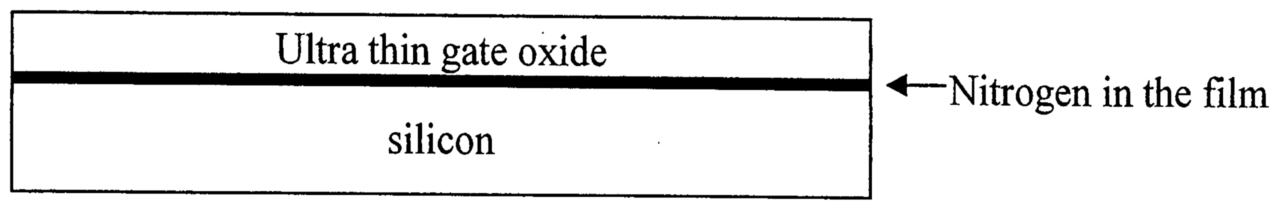
Sundar Narayanan

Krishnaswamy Ramkumar

What is the problem?

Ultra thin gate oxides with nitrogen incorporation, cannot be monitored for nitrogen incorporation using conventional metrology tools.

This is because of the low amount of nitrogen present in the oxide. This does not change the film properties of the thin oxide to a level where the optical methods can measure them.



SIMS is the only method of accurately determining nitridation efficiency.

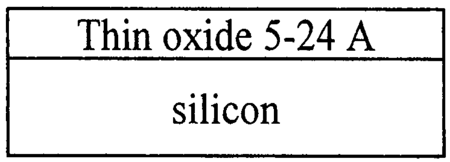
Disadvantages of current method

- SIMS cannot be done in a manufacturing facility to test production lots and get a pass fail criteria instantly and non destructively.
- Cost of SIMS is prohibitive.
- Method not condusive for SPC (statistical process control).

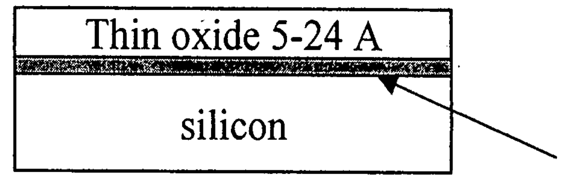
Proposed Method

The proposed method involves growing the gate dielectric with the following sequence.

1. Grow thin oxide in Furnace or RTO

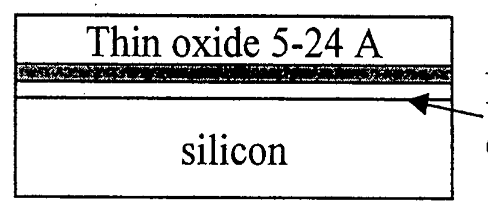


2. Nitriding thin oxide using 99.9 or 9.9999 % NO gas in Furnace or RTO



2-4 A increase with nitridation

3. Reoxidation of the nitrided oxide using pure Oxygen at 800 C to 1025 C in a furnace or RTO.



Increase of 1-4 A due to oxidation.

Wafer description	Before 2nd oxidation	After 2nd oxidation
With Nitrogen	22.43 A	26.6 A
Without Nitrogen	23.19 A	**101.10 A**

Advantages / claims of new method

With this process we have a self monitoring process for the nitrogen incorporation.
There is no need for any other metrology tool or step.
The process enables us to use Statistical Process control on % Nitrogen in a manufacturing fab and can help detect instant nitridation failure.
We can do the process in the furnace or single wafer tool and get improved mobility due to the addition of oxide at the gate dielectric silicon interface.
The entire process can be done in the same recipe in one tool or can be done in two different tools (a furnace and a single wafer tool).
By changing the second oxidation time and temperature it is possible to get a good resolution on the nitrogen content of the thin gate dielectric and do SPC on the % N as well.